

REMARKS/ARGUMENTS

Claim rejections 35 USC § 103

Claims 1-21 were rejected under 35 USC 103(a) as being allegedly unpatentable over Profit, Jr U.S. Pat. No. 5,911,059 (hereinafter, Profit) in view of “DEBUG” as described in “A DEBUG Tutorial” by Daniel B. Sedory (hereinafter Sedory) and in further view of “Microsoft PressPass – Microsoft Files Summary Judgment Motions” by Microsoft (hereinafter Microsoft). The Applicants respectfully traverse the rejection.

Amended independent Claim 1 recites (emphasis added):

“In-Circuit Emulation system, comprising:

...;

a virtual microcontroller running in lock-step synchronization with the microcontroller by executing the same instructions using the same clocking signals between said microcontroller and said virtual microcontroller;

a gatekeeper circuit ...; and

... halt commands and requests for data ... regulated by the gatekeeper circuit to assure that emulator operations are not disrupted.”

Accordingly, the virtual microcontroller and the microcontroller execute instructions in lock-step by executing the same instructions using the same clock signals. Furthermore, since the two processors operate in lockstep, there is no need to provide bus arbitration, framing, or other protocol overhead to effect the communication between the microcontroller and the virtual microcontroller.

Profit discloses that the communication interface performs two primary functions, one of which is resynchronization of the target program and target circuitry on a periodic basis. (See Profit, col. 7, lines 31-52). As such, Profit suggests that the target program and target circuitry go out of synch, hence requiring resynchronization using a communication interface. Accordingly, Profit requires bus arbitration, framing and other protocol overhead to effect the communication between the microcontroller and the virtual microcontroller. (See Profit, Figures 7, 8 and 9). Profit further suggests that setting the time interval to zero would cause synchronization to occur at the execution of each instruction. (See Profit, col. 11, lines 40-43). Accordingly, Profit teaches synchronization by setting the time interval to zero instead of lockstep synchronization by virtue of identical operations and shared clock signals.

Newly amended independent Claim 1 distinguishes over Profit by reciting “a virtual microcontroller running in lock-step synchronization with the microcontroller by executing the same instructions using the same clocking signals between said microcontroller and said virtual microcontroller.” In contrast, Profit’s synchronization is achieved by setting the time interval to zero instead of lockstep synchronization by running identical operations and a shared clock signals. Furthermore, Profit uses additional circuitry (e.g., communication interface) in order to resynchronize the target program and the target circuitry, requiring bus arbitration, framing and other protocol overhead to effect the

communication between the microcontroller and the virtual microcontroller whereas in independent Claim 1 no additional circuitry is used to run instruction in lock-step and as such there is no need to provide bus arbitration, framing, or other protocol overhead in order to communicate between the microcontroller and the virtual microcontroller. As such, Profit does not disclose executing the same instructions using the same clocking signals between said microcontroller and said virtual microcontroller, as claimed.

Profit further, discloses that when the target program needs to access the simulated target circuit, the RUN/HALT state machine provides a signal causing the processor to halt execution and immediately after providing TBW INTERRUPT. (See Profit, col. 9, lines 40-60). Profit also discloses a processor is halted when a synchronization of the target program and the simulated target circuit is required where the state machine provides the RUN/HALT signal when it receives the TBW INTERRUPT. (See Profit, col. 9, lines 62-67). As such, Profit halts the program as soon as access to the simulated target circuit is needed or as soon as synchronization is required.

Independent Claim 1 further distinguishes over Profit by reciting halt commands and requests for data regulated by the gatekeeper circuit to assure that emulator operations are not disrupted. In contrast, Profit discloses that the program is halted as soon as access to the simulated target circuit is needed or as soon as synchronization is required whereas in independent Claim 1 a halt

command is regulated to assure that emulator operations are not disrupted. As such, Profit does not disclose halt commands and requests for data regulated by the gatekeeper circuit to assure that emulator operations are not disrupted, as claimed.

The rejection admits that Profit does not explicitly disclose requests for data from the virtual microcontroller are passed through and regulated by the gatekeeper circuit. In order to overcome this defect, the rejection relies on the recited Microsoft reference. The Applicants do not understand Microsoft to remedy this defect.

Accordingly, Profit, alone or in combination with Microsoft does not render newly amended independent Claim 1 obvious, under 35 USC 103(a) because the combination does not disclose executing the same instructions using the same clocking signals between said microcontroller and said virtual microcontroller nor does it teach halt commands and requests for data regulated by the gatekeeper circuit to assure that emulator operations are not disrupted, as claimed. As such, allowance of independent Claim 1 is earnestly solicited.

Claims 2-12 depend from independent Claim 1 and are each patentable over the combination of Profit and Microsoft, under 35 USC 103(a), at least for the same reasons that independent Claim 1 is patentable.

Moreover, Claim 2 distinguishes over Profit by reciting gatekeeper clock running independent of the microcontroller clock. Profit discloses that a clock 242 drives the latch control circuit 248 where this clock is typically the same clock, which drives the processor 204. (See Profit, col. 9, lines 28-30). Accordingly, the clock disclosed in Profit does not run independent of the microcontroller but is rather the same clock. As such, Profit does not disclose and in fact teaches away from gatekeeper clock running independent of the microcontroller clock, as claimed.

As per Claim 3, the rejection states that Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to placing it in a sleep state and that placing a microcontroller into a sleep state reasonably apprise that the microcontroller is in a sleep state. However, in order to reasonably apprise that the microcontroller is in a sleep state, necessarily requires halting the microcontroller whereas in Claim 3 halting the microcontroller is irrelevant to detection of sleep state.

As per Claims 4-6, Profit does not disclose nor suggests determining whether microcontroller is in the sleep state as discussed above.

As per Claim 7, Profit does not disclose queuing a break to the microcontroller and the virtual microcontroller because in Profit the program halts immediately as discussed above, thereby circumventing the need for queuing a

break. As such, Profit teaches away from queuing a break to the microcontroller and the virtual microcontroller, as claimed.

As per Claims 9-10, Claims 9-10 depend from Claim 7 and are each patentable at least for the same reasons that Claim 7 is patentable.

As per Claim 11, Profit discloses that hardware simulator and processor model shell typically run on a host computer, which typically contains a software package for designing the simulation of the target circuitry, and that software debugging tools are typically contained on the host computer. (See Profit, col. 6, lines 49-60). As such, Profit teaches away from using a gatekeeper for permitting access to registers and memory locations because Profit suggests that software package for designing and debugging are typically contained on the host computer and not the gatekeeper. As such, Profit does not disclose a gatekeeper for permitting access to registers and memory locations, as claimed.

Accordingly, Claims 2-12 are not rendered obvious over the combination of Profit and Microsoft, under 35 USC 103(a). As such, allowance of Claims 2-12 is earnestly solicited.

Independent Claim 13 is similar in scope to that of independent Claim 1. Accordingly, independent Claim 13 is not rendered obvious, under 35 USC 103(a) at least for the same reasons that independent Claim 1 was not rendered obvious. As such, allowance of independent Claim 13 is earnestly solicited.

Claims 14-20 depend from independent Claim 13 and include the limitations of independent Claim 13. Accordingly, Claims 14-20 are patentable at least for the same reasons that independent Claim 13 is patentable. As such, allowance of Claims 14-20 is earnestly solicited.

Claim 21 recites the method employed by a system combining the limitations of Claims 5-6 and 8-11 as discussed above. Accordingly, independent Claim 21 is not rendered obvious under 35 USC 103(a) over the combination of Profit and Microsoft. As such, allowance of Claim 21 is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of these rejections under 35 U.S.C. §103.

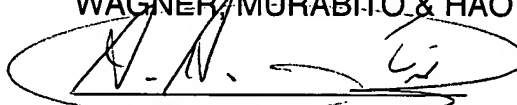
CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-21 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-21 overcome the rejections of record and, therefore, allowance of Claims 1-21 is earnestly solicited.

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Dated: Jan 9, 2005

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

A handwritten signature in black ink, appearing to read 'A. Tabarrok', is enclosed within a hand-drawn oval.

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